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Appl. No. 10/024,904***Remarks***

Reconsideration of this Application is respectfully requested. Upon entry of the foregoing Amendment to the Claims, claims 1-21 are pending in the application, of which claims 1, 8, and 15 are independent. By the foregoing Amendment, claims 1-3, 6, 8-10, 15-17, and 20 are sought to be amended. No new matter is embraced by this amendment and its entry is respectfully requested. Based on the above Amendment and the remarks set forth below, it is respectfully requested that the Examiner reconsider and withdraw all outstanding rejections.

The Specification

The Examiner, on page 2 of the Office Action, has requested Applicants' cooperation in correcting any errors of which Applicants may become aware of in the Specification. Paragraphs [0013], [0014], [0015], [0016], [0017], and [0019] have been amended to correct minor typographical and editorial errors.

The Title

The Examiner, on page 2 of the Office Action, has indicated that the title of the invention is not descriptive. Applicants have amended the title of the invention to provide a more descriptive title.

Rejection under 35 U.S.C. § 102

The Examiner, on page 3 of the Office Action, states that claims 1-21 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Application Pub. No.

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2002/0169990 A1 to Sherburne, JR (hereinafter "Sherburne"). Applicant respectfully traverses this rejection. Based on the remarks set forth below, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

To anticipate a claim of a pending application, a single reference must disclose each and every element of the claimed invention. *Hybritech Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 1397 (Fed. Cir. 1986). The exclusion of a claimed element from the single source is enough to negate anticipation by that reference. *Atlas Powder Co. v. E.I. du Pont de Nemours & Co.*, 750 F.2d 1569, 1574 (Fed. Cir. 1984).

With respect to independent claims 1, 8, and 15, the Examiner states that Sherburne teaches every element of these claims. Applicant respectfully disagrees.

Contrary to the present invention, Sherburne does not teach or suggest every element of Applicant's invention. For example, referring to independent claim 1, Sherburne does not teach or suggest at least the following claimed elements:

- determining a first memory buffer level for at least one memory buffer providing data to digital circuitry,
- determining a second memory buffer level for the at least one memory buffer, the second memory buffer level being set greater than the first memory buffer level,
- comparing data buffer levels in memory with the first and second memory buffer levels.

Unlike the present invention, Sherburne does not appear to teach or suggest determining a first memory buffer level, determining a second memory buffer level, and comparing data buffer levels in memory with the first and second memory buffer levels. Instead, Sherburne discloses a buffer as a FIFO (first-in, first-out memory circuit). *Sherburne*, page 3, paragraph [0026]. The FIFO uses a dual port RAM, a write address counter, a read address counter, and a coincidence detect circuit. *Id.* "The coincidence

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detect circuit recognizes the state of the dual port RAM according to the data write signal, the data read signal, the write address signal and the read address signal and outputs a FULL signal or a EMPTY signal.” *Sherburne*, page 3, paragraph [0027], lines 8-12. Thus, *Sherburne* does not teach determining a first memory buffer level, determining a second memory buffer level, and comparing data buffer levels in memory with the first and second memory buffer levels. Instead, *Sherburne* teaches a FIFO having a coincidence detect circuit that uses data write and read signals along with write address and read address signals to recognize the state of the dual port RAM and output one of a FULL or EMPTY signal to indicate the data level of the FIFO.

For at least these reasons, *Sherburne* does not include each and every element of Applicants’ claimed invention recited in independent claim 1, and the claims that depend therefrom (claims 2-7). Applicant respectfully submits that claims 1-8 are not anticipated by *Sherburne*.

Independent claim 8 recites elements similar to the elements of claim 1. Thus, for at least the reasons stated above, claim 8 and the claims that depend therefrom (claims 9-14), are not anticipated by *Sherburne* as well.

With respect to independent claim 15, *Sherburne* does not teach or suggest at least the following claimed element: “a memory buffer monitoring unit to compare a memory buffer level to a first and second memory buffer level for at least one memory buffer providing data to digital circuitry, the second memory buffer level being set greater than the first memory buffer level.” As indicated above, *Sherburne* does not teach or suggest comparing a memory buffer level to a first and second memory buffer level for at least one memory buffer.

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For at least these reasons, Sherburne does not include each and every element of Applicants' claimed invention recited in independent claim 15, and the claims that depend therefrom (claims 16-21). Applicant respectfully submits that claims 15-21 are not anticipated by Sherburne.

Therefore, independent claims 1, 8, and 15, and the claims that depend therefrom, are patentable over Sherburne. Reconsideration and withdrawal of this rejection is respectfully requested.

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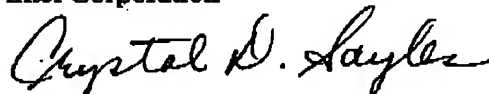
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Appl. No. 10/024,904**Conclusion**

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider all currently outstanding rejections and that they be withdrawn. It is believed that a full and complete response has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Response is respectfully requested.

Respectfully submitted,

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